REMARKS

Claims 1-14, 16-21 and 23-31 are pending in the application. Claims 20, 21, 23 and 24 are allowed. Claims 1-14, 25-31 are rejected under 35 U.S.C. §102(e) as being anticipated by Winters (U.S. 6,292,818). Applicants gratefully acknowledge the Office Action's indication that claims 16-19, 20-21 and 23-24 contain allowable subject matter.

A. Claims 1-9 are allowable over Winters and the art of record

Applicant submits that the cited prior art does not teach, suggest, or disclose "[a]n apparatus comprising a symmetric differential domino carry generate circuit *having true inputs and compliment inputs which both have a load*, wherein the load for the true inputs is equal to the load for the compliment inputs" (e.g., as described in claim 1).

In its rejection, the Office Action cites generally to Figure 6 as disclosing the relevant limitations, with no further specific citation. *See* Office Action, page 3, line 5. In the Response to Arguments section, the Office Action states that the cited reference clearly discloses in Figure 6 the true inputs (e.g. A1H, B1H and C1H) (the "H set") and the complement inputs (e.g., A1L, B1L and C1L) (the "L set"), further claiming they are complements to each other having equal load. Applicants disagree.

There is no teaching, suggestion or disclosure in the cited reference that the two input sets "H" and "L", are compliments of each other. Figure 6 is described in the three paragraphs spanning column 5, line 35 to column 6 line 10. The first paragraph describes a schematic diagram of the propagate/generate logic block shown in Figure 3. The second paragraph describes the dynamic logic gate comprised of circuits 21A and 21B used to generate and

propagate static outputs. It further states that: "Nodes identified in Fig. 6 with identical reference numbers are coupled together". *See* column 5, line 52. However, there is no further description of the nodes, and there is no suggestion whatsoever that any inputs are complimentary as described in the embodiment of claim 1. The last paragraph describes the manner in which the precharged nodes are charged by PMOS FETs in response to a clock signal that is high/low. Applicants maintain however, there is no suggestion that any inputs, including the alleged the "H" set and the "L" set, *are complimentary* (or even that they have an equal load) as described in the embodiment of claim 1.

Therefore, Applicants submit that the Examiner's claim that these two input sets are compliments to each other is completely unsupported by the reference. Applicants note that in the initial rejection, despite the Office Action's claims, there was no specific citation to any section of Winters, but rather a generic reference to Figure 6 as a whole. In the recent Office Action and its Response, again there is no reference to a specific place in Winters as disclosing the relevant limitations, but a general citation supplemented by an unsupported assertion.

In light of the arguments made above, and the need for each rejection to be taught, suggested or disclosed by the reference, Applicants submit that the Winters reference is inadequate to support a proper 35 U.S.C. 102(e) reference, and the rejection should be withdrawn. Independent claim 4 contains similar allowable limitations. Claims 2-3 and 5-9 are allowable for depending from allowable base claims.

B. Claims 10-14 are allowable over Winters and the art of record

Next, Applicants submit the cited reference does not teach, suggest, or disclose at least "[a]n apparatus comprising...a fourth transistor with a drain connected to the source of the third

transistor and a source connected to the current input, and a fifth transistor with a drain connected to the second output and a source connected to the drain of the fourth transistor..." (e.g., as described in claim 10).

In the response section of the most recent Office Action (*see* Page 8, paragraph b), the Office Action claims that Figure 6 discloses first, second, third, fourth and fifth transistors wherein a fourth transistor with a drain connected to the source of the third transistor (e.g., transistor on the left for receiving A1L) and a fifth transistor (e.g., transistor for receiving A1H) with a drain connected to the second output (e.g., either 25/26 as EVAL) and a source connected to the drain of the fourth transistor. Applicants disagree.

As described in the summary of the description of Figure 6 detailed above, there is no mention of any transistors *connected to drains*. Moreover, Applicants note that while the Office Action cites elements A1H, B1H... etc. as allegedly disclosing transistors, there is no specific citation to the drains corresponding to the transistors as specifically recited in the embodiment of claim 10. The Office Action cites the A1H, B1H ...etc., which as asserted above, are not described in the specification at all as being in conjunction with a drain. Moreover, cited elements 25/26 are PMOS FET (*see* column 5, line 58), which also are not accompanied by any descriptions of associated drains. Lastly, an examination of Figure 6 of Winters clearly indicates the lack of any associated drains with any of the elements described in Figure 6.

In order to support a proper 35 U.S.C. 102(e) rejection, each and every limitation of the claim must be found in the cited reference. However, since the Winters does not teach, disclose or even suggest at least the use of transistors in association with drains at all, the rejection is improper and should be withdrawn. Dependent claims 11-14 are allowable as depending from an allowable base claim.

C. Claims 25-30 are allowable over Winters and the art of record

Lastly, Applicants submit the cited reference does not teach, suggest, or disclose "[a] method comprising: ....receiving at a second evaluation block three compliment input values, wherein the compliment input values are the compliment of the true input values; processing the compliment input values at the second evaluation block to provide a carry generate value at a first output... and processing the true input values at the first evaluation block to provide the compliment of the carry generate value at a second output ..." (e.g., as described in claim 25).

Applicants submit the outputs of the three transistors in FIG. 6 that have inputs C1L and VDD, C1H and VDD, and B1L are used to generate both NSUM and SUM. Thus, because they are used to generate both values, neither is part of a "second evaluation block to provide a carry generate value" or a "first evaluation block to provide the compliment of a carry generate value." Similarly, the remaining transistors in the circuit are neither part of a first evaluation block or second evaluation block as recited in claim 25 *because these transistors cannot provide a carry generate value or a compliment carry generate value* without the aforementioned three transistors in FIG. 6 that have inputs C1L and VDD, C1H and VDD, and B1L.

In its response, the Office Action argues that the cited reference includes processing compliment input values at a second evaluation block to provide a carry generate value (e.g., 23 for carry as in 21A), or processing true input values at a first evaluation block to provide the compliment of a carry generate value (e.g., 22 for carry as in 21A because the structure for sum and carry are mirror). Applicants disagree.

The Office Action's assertion that 23 and 22 as carries for 21A. However, this is unsupported by the Winters reference. The Winters reference discloses elements 22 and 23 only

as "dynamic precharged nodes", with no reference to a carry operation or any equivalent thereof. Applicants submit that this is insufficient to support a proper 35 U.S.C. 102(e) rejection. The Office Action's assertion that the elements 22, 23 are carry operations is completely without support from the Winters reference itself. In addition, as argued previously, Figure refers to NSUM and SUM values without any reference to a carry value. Applicants submit that, in order to be a proper rejection, there must be at least a teaching, suggestion or disclosure from the reference itself indicating that a carry generate value is being provided. There is none.

Therefore, Applicants submit since each and every limitation is not found in the Winters reference, 35 U.S.C. 102(e) rejection of claim 25 is lacking and should be withdrawn. Claims 26-30 are allowable for depending from an allowable base claim.

Conclusion

For at least all the above reasons, the Applicants respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. **11-0600**.

Respectfully submitted,

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